memory to change their order and secondarily decoding the interleaved signals. Independent claim 1 also recites deinterleaving the secondarily decoded signals and storing the deinterleaved signals in the specific address space of the memory, wherein the interleaving, the secondarily decoding, and the deinterleaving are implemented simultaneously.

Van Stralen does not teach or suggest all the features of independent claim 1. More specifically, independent claim 1 specifically recites storing the primarily decoded signals in a specific address space of a memory, interleaving the primarily decoded signals stored in the memory and storing the deinterleaved signals in the specific address space of the memory. Van Stralen does not teach or suggest these features. Van Stralen discloses a top code memory 16, a bottom code memory 20 and a probability estimate memory 24. However, there is no suggestion in Van Stralen for storing primarily decoded signals in a specific address space of a memory and also storing the deinterleaved signals in the specific address space of the memory. Merely because signals may be stored in one memory, this does not suggest storing both types of signals in a specific address space of a memory. See paragraphs [20]-[21] of the present specification, for example.

Additionally, Van Stralen does not teach or suggest that the interleaving, the secondarily decoding and the deinterleaving are implemented simultaneously. The Office Action asserts on pages 3-5 that Van Stralen does disclose "implemented simultaneously." The Office Action appears to make assertions without any actual basis in the reference. More specifically, the Office Action generally states (when making a generalization as compared to a car assembly) that "all of

these steps are implemented simultaneously to achieve the overall desired operation." However, Van Stralen does not state that various operations of Van Stralen are "implemented simultaneously." Rather, the Office Action's basis for this assertion is based on applicant's own disclosure and not based on the teachings of Van Stralen. Applicant further submits that this feature is also not inherently provided within Van Stralen.

The Office Action also asserts that Van Stralen's operation occurs on a stream of data and that turbo decoding is continuously processing a feed of data with all parts implemented simultaneously. Applicant respectfully submits that Van Stralen does not teach this alleged feature and that the Office Action's assertion is without any basis in the prior art. See also paragraphs [52]-[53] where it is discussed how the speed of the turbo decoding can be reduced. The described methodology therefore improves over other turbo decoding techniques. This shows that not all turbo decoding occurs as alleged in the Office Action. The Office Action's argument with respect to the stream of data therefore is not proper and/or does not show anticipation of the claimed features.

Still further, the Office Action (on the paragraph bridging pages 4-5) states that each of the input lines is a disparate and independent entity and operations performed on each of the input lines would necessarily require processing to be "implemented simultaneously." However, the claimed features are more than just three features being performed simultaneously. That is, independent claim 1 specifically recites the interleaving (relating to the previously recited interleaving based on specific signals), the secondarily decoding (relating to the previously recited

secondarily decoding based on specific signals), and the deinterleaving (relating to the previously recited deinterleaving based on specific signals. Thus, the Office Action's arguments do not teach the specifically claimed features.

For at least the reasons set forth above, Van Stralen clearly does not teach that the interleaving, the secondarily decoding and the deinterleaving are implemented simultaneously, as is explicitly recited in independent claim 1.

Applicant further directs the Examiner's attention to paragraphs [0050] and [0020] (last three lines) of the present application relating to the deinterleaving being performed with the secondary MAP decoding because the data generated from the second MAP decoder 103 is stored in the address region of the memory 106. As stated above, Van Stralen does not teach or suggest this specific memory address of the memory. Van Stralen also does not teach or suggest the "implemented simultaneously" feature recited in independent claim 1. Accordingly, Van Stralen does not teach or suggest all the features of independent claim 1. Thus, independent claim 1 defines patentable subject matter.

Independent claim 6 recites various features, including storing the primarily decoded signals in a specific address space of a memory, interleaving the primarily decoded signals stored in the memory and storing the deinterleaved signals in a predetermined region of the memory, wherein the interleaving, the secondarily decoding and the deinterleaving are implemented simultaneously. For at least similar reasons as set forth above, Van Stralen does not teach or

suggest all these features of independent claim 6. Thus, independent claim 6 defines patentable subject matter.

Independent claim 11 recites storing the primarily decoded composite signals in a specific address space of a memory, interleaving the signals stored in the memory and storing the deinterleaved signals in the specific address space of the memory, wherein the interleaving, the secondarily decoding and the deinterleaving are implemented simultaneously. For at least similar reasons as set forth above, Van Stralen does not teach or suggest all these features of independent claim 11. Thus, independent claim 11 defines patentable subject matter.

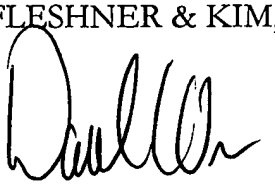
For at least the reasons set forth above, each of independent claims 1, 6 and 11 define patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-4, 6-9 and 11-14 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this,

concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



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